**Studytonight – CAO test 6 – Aditya Jain**

1. **The physical memory is not as large as the address space spanned by the processor.**

**a) True**  
b) False

Explanation: This is one of the main reasons for the usage of virtual memories.

1. **The main purpose of having memory hierarchy is to**a) Reduce access time  
   b) Provide large capacity  
   c) Reduce propagation time  
   **d) Reduce access time & Provide large capacity**

Explanation: By using the memory Hierarchy, we can increase the performance of the system.

1. **The program is divided into operable parts called as \_\_\_\_\_\_\_\_\_**a) Frames  
   b) **Segments**  
   c) Pages  
   d) Sheets

Explanation: The program is divided into parts called as segments for ease of execution.

1. **The binary address issued to data or instructions are called as \_\_\_\_\_\_**

a) Physical address  
b) Location  
c) Relocatable address  
d) **Logical address**

Explanation: The logical address is the random address generated by the processor.

1. **The key factor/s in commercial success of a computer is/are \_\_\_\_\_\_\_\_**a) Performance  
   b) Cost  
   c) Speed  
   **d) Both Performance and Cost**

Explanation: The performance and cost of the computer system is key decider in the commercial success of the system.

1. **An effective to introduce parallelism in memory access is by \_\_\_\_\_\_\_**

a) **Memory interleaving**b) TLB  
c) Pages  
d) Frames

Explanation**: Memory Interleaving** divides the memory into modules. For detailed explanation, you may visit <https://www.studytonight.com/computer-architecture/interleaved-memory.php>

1. **\_\_\_\_\_\_ translates logical address into physical address.**

**a) MMU**  
b) Translator  
c) Compiler  
d) Linker

Explanation: A **Memory Management Unit (MMU)**, sometimes called **Paged Memory Management Unit (PMMU)**, is a computer hardware unit having all memory references passed through itself, primarily performing the translation of virtual memory addresses to physical addresses.

1. **The main aim of virtual memory organisation is**

a) To provide effective memory access  
b) To provide better memory transfer  
c) To improve the execution of the program  
**d) All of the mentioned**

1. **The techniques which move the program blocks to or from the physical memory is called as \_\_\_\_\_\_**a) Paging  
   b) **Virtual memory organisation**c) Overlays  
   d) Framing

Explanation: By using this technique the program execution is accomplished with usage of less space.

1. **\_\_\_\_\_\_\_\_\_\_is used to implement virtual memory organisation.**

a) Page table  
b) Frame table  
c) **MMU**  
d) None of the mentioned

Explanation: A **Memory Management Unit (MMU)**, sometimes called **Paged Memory Management Unit (PMMU)**, is a computer hardware unit having all memory references passed through itself, primarily performing the translation of virtual memory addresses to physical addresses.

1. **The virtual memory basically stores the next segment of data to be executed on the \_\_\_\_\_\_\_\_\_**

**a) Secondary storage**  
b) Disks  
c) RAM  
d) ROM

1. **The DMA doesn’t make use of the MMU for bulk data transfers.**

**a) True**b) False

Explanation: The DMA stands for Direct Memory Access (DMA), in which a block of data gets directly transferred from the memory **without** making use of MMU.

1. **The main objective of the computer system is**

a) To provide optimal power operation  
**b) To provide best performance at low cost**c) To provide speedy operation at low power consumption  
d) All of the mentioned

Explanation: An optimal system provides best performance at low costs.

1. **The associatively mapped virtual memory makes use of \_\_\_\_\_\_\_**

**a) TLB**  
b) Page table  
c) Frame table  
d) None of the mentioned

Explanation: A **Translation Lookaside Buffer (TLB)** is a memory cache that stores recent translations of virtual memory to physical addresses for faster retrieval.

When a virtual memory address is referenced by a program, the search starts in the CPU. First, instruction caches are checked. If the required memory is not in these very fast caches, the system has to look up the memory’s physical address. At this point, TLB is checked for a quick reference to the location in physical memory.

1. **The performance of the system is greatly influenced by increasing the level 1 cache.**a) **True**  
   b) False

Explanation: The **L1 cache** is built using larger transistors and wider metal tracks, trading off space and power for speed. The higher level caches are more tightly packed and use smaller transistors, thereby greatly influencing the performance of the system.